[SPECIFICATION]

[Title of the Invention]

LIQUID CRYSTAL DISPLAY DEVICE

[Brief Description of the Drawings]

Fig. 1 is a block diagram illustrating the circuit structure of a liquid crystal display according to a prior art;

Fig. 2 is a block diagram of a PCB module for the liquid crystal display device shown in Fig. 1;

Fig. 3 is a block diagram of another PCB module for the liquid crystal display device shown in Fig. 1;

Fig. 4 is a block diagram of a PCB module for a liquid crystal display device according to a preferred embodiment of the present invention;

Fig. 5 illustrates an arrangement of picture data supplied from source drivers of the PCB module shown in Fig. 4; and

Fig. 6 illustrates a way of partitioning a liquid crystal panel for the liquid crystal display device shown in Fig. 4

[Detailed Description of the Invention]

[Object of the invention]

[Field and related art of the invention]

The present invention relates to a liquid crystal display device and, more particularly, to a liquid crystal display device which is provided with a printed circuit board (PCB) module adapted for wide screen and high resolution.

Generally, a liquid crystal display device includes a liquid crystal display module with a liquid crystal panel where liquid crystal cells are arranged between two glass substrates in a matrix form, and a backlight unit installed at the rear of the liquid crystal panel, a PCB module installed at the rear of the backlight unit to drive the liquid crystal panel, and a case covering the liquid crystal display module and the PCB module to protect them. The PCB module is a driving circuit that receives picture data of red (R), green (G) and blue (B) and synchronization signals from the outside, and processes them to generate picture signals, scanning signals and timing control signals. The PCB module transmits the generated signals to the liquid crystal panel such that the latter can display the desired images such as computer image, TV image etc., in a stable manner. Such a PCB module is provided with a plurality of PCBs, and flexible printed cables (FPCs) interconnecting the PCBs for signal transmission.

Fig. 1 is a block diagram illustrating the circuit structure of a liquid crystal display device according to a prior art. As shown in Fig. 1, the PCB module for a display device bearing relatively lower resolution of SVGA (600 * 800) includes a main PCB 10, a gate driver PCB 20, and a source driver PCB 30 or 40. The main PCB 10 receives picture data of R, G and B and synchronization signals from the outside, and processes them by way of a timing controller (T-con) such that they are adapted for the structure of a liquid crystal panel 50. The timing controller is a custom IC in the form of a flat pin grid array (FPGA).

Gate driver IC tape automated bonds (TABs) are attached to the gate driver PCB 20 to receive gate driver control signals 60 and 61 from the main PCB 10, and to supply scanning signals to the liquid crystal panel 50 based on the received control signals 60 and 61. Source driver IC TABs are attached to the source driver PCB 30 or 40 to receive source driver control signals 70 and 71 from the main PCB 10, and to supply picture signals to the liquid crystal panel 50 based on the received control signals 70 and 71.

The PCB module further includes an FPC for transmitting the gate driver control signals 60 and 61 from the main PCB 10 to the gate driver PCB 20, and an FPC for transmitting the source driver control signals 70 and 71 from the main PCB 10 to the source driver PCB 30 or 40. In case the main PCB 10 is separated into two or more portions, other FPCs may be provided to interconnect the separated portions of the main PCB 10.

As the liquid crystal display device has been developed to bear wide screen and high

resolution of XGA (768 * 1024), SXGA (1024 * 1280), or UXGA (1200 * 1600), a dual bank typed PCB module is mainly used for such a display device in consideration of width of data lines placed at a bottom substrate of the liquid crystal panel 50, space for driver IC TABs attached to the source driver PCB 30 or 40 and to the bottom substrate of the liquid crystal panel 50, and partitioned driving due to the high speed of data processing. In the dual bank typed PCB module, two source driver PCBs are installed at the rear of the liquid crystal panel 50 up and down to supply picture signals thereto from the top and the bottom.

Figs. 2 and 3 illustrate the structure of a dual bank typed PCB module for a liquid crystal display device, respectively.

As shown in Fig. 2, source driver PCBs 110 and 120 are installed at the rear of a liquid crystal display module 100 up and down such that they are connected to an I-shaped main PCB 140 via FPCs 150 and 170, respectively. A gate driver PCB 130 is connected to the main PCB 140 via an FPC 160 side by side. The main PCB 140 is provided with a timing controller to generate various kinds of data and control signals, and supply them to the source driver PCBs 110 and 120 and the gate driver PCB 130 via the FPCs 150 to 170.

As shown in Fig. 3, source driver PCBs 210 and 220 are installed at the rear of a liquid crystal display module 200 up and down such that they are connected to three main PCBs 240 to 242 via FPCs 250 and 280, respectively. A gate driver PCB 230 is connected to the main PCB 240 via an FPC 290 side by side. The main PCBs 240 to 242 are provided with a timing controller to generate various kinds of data and control signals, and supply them to the source driver PCBs 210 and 220 and the gate driver PCB 230 via the FPCs 250 to 290.

However, in the usual dual bank typed PCB module shown in Fig. 2, the transmission of the picture data is delayed at the right screen portion when viewed from the front side so that normal display cannot be made, even though the picture data is driven in a double-partitioned way in the liquid crystal panel bearing a screen size of 20 inch or more, and high resolution. In order to overcome such a problem, as shown in Fig. 3, it is proposed that three separate main PCBs 240 to 242 should be introduced while being interconnected via two FPCs 260 and 270. A space for mounting driver IC TABs, signal lines to be supplied to the drive IC TABs, resistors and condensers for supplying appropriate bias to various signal voltages are provided at the source driver PCBs 210 and 220, and the main PCBs 240 to 242 are designed in consideration of intersignal coupling, noise, and electromagnetic interference (EMI) such that the required signal transmission can be made within the range of tolerance. However, even in such a structure, signal delay or distortion is liable to be generated due to the delay factor intrinsic to resistance capacitance (RC) in the process of interconnecting the PCBs by way of the FPCs 260 and 270. The RC may accrue to the combination resistance of the PCB connector and the FPC connector, and other parasitic capacitance. Consequently, the signals applied to the source driver PCBs 210 and 220 are not timing-controlled in a stable manner so that setting and holding of the picture data become to be inappropriate for

displaying, resulting in serious display failure accompanied with screen noise and line defect.

Meanwhile, the usual liquid crystal display screen is formed with a rectangular shape where the ratio of the horizontal length to the vertical length is 4:3, or 16:9. However, in near future, it is expected that the display screen for medical equipment and radar where screen size and resolution are heightened with an enlarged vertical length may be formed with a square shape. Accordingly, the number of horizontal lines per frame is increased in signal processing and hence, one horizontal synchronization signal cycle becomes shortened so that the period of time for processing the picture data is reduced, resulting in decreased timing margin. In this respect, it is required to develop a technique of processing the picture data in the range of tolerance for signal delay and distortion while preventing screen noise, coupling, and EMI.

[Object of the invention]

It is an object of the present invention to provide an arrangement method of a PCB module which can reduce signal delay and distortion in driving a liquid crystal panel bearing wide screen and high resolution.

[Summery of the invention]

In order to achieve this object, the liquid crystal display device includes dual bank typed source driver PCBs installed at the top and the bottom of a liquid crystal panel, a gate driver PCB, and a staple-shaped main PCB formed in a body with top and bottom portions proceeding in the horizontal direction and a side portion proceeding in the vertical direction. The top and the bottom portions of the main PCB axially meet the side portion of the main PCB at a predetermined angle. A timing controller is mounted at the main PCB to process signals input from the outside and generate driving signals. The main PCB transmits the relevant driving signals to the respective source driver PCBs and the gate driver PCB.

The top and bottom portions of the main PCB axially meet the side portion of the main PCB substantially at a right angle. Alternatively, the top and the bottom portions of the staple-shaped main PCB may axially meet the side portion of the main PCB at an acute angle, or an obtuse angle.

The top and bottom portions of the staple-shaped main PCB have an axial length of one second or more of the liquid crystal panel.

The respective top and bottom portions of the staple-shaped main PCB are connected to the corresponding source driver PCBs via one or more FPCs to transmit the relevant driving signals to the source driver PCBs.

The side portion of the staple-shaped main PCB is connected to the gate driver PCB via one or more FPCs to transmit the relevant driving signals to the gate driver PCB. The timing controller is positioned at the side portion of the staple-shaped main PCB.

Accordingly, in the liquid crystal panel with a dual bank typed PCB module according to an embodiment of the present invention, the source driver is partitioned into two parts and installed at the rear of the liquid crystal display module up and down to supply the picture data to the liquid crystal

display module. In driving the liquid crystal panel in a double or quadruple-partitioned way, the staple-shaped main PCB minimizing signal delay and distortion is used. Accordingly, such a main PCB can be well adapted for driving the liquid crystal panels with a large screen and high resolution.

Preferred embodiments of the present invention will be described in detail with reference to the accompanying drawings. An IPS LCD according to an embodiment of the present invention is described now.

Fig. 4 is a block diagram of a liquid crystal display device according to a preferred embodiment of the present invention.

As shown in Fig. 4, the liquid crystal display device includes a liquid crystal display module 300. First and second source driver PCBs 310 and 320 are installed at the rear of the liquid crystal display module 300 up and down such that they are connected to a substantially stapled-shaped main PCB 340 via first to fourth source FPCs 350 to 380. The main PCB 340 is installed at the rear of the liquid crystal display module 300 in one body. A gate driver PCB 330 is connected to the main PCB 430 via gates 390 and 400 side by side. The main PCB 340 is applied picture data etc. from an external device, processes them using a timing controller, generates various kinds of data and control signals, and supplies them to the source driver PCBs 310 and 320 and the gate driver PCB 330 via the FPCs 350 to 400.

The dual bank typed PCB module according to an embodiment of the present is to drive the picture data in a double-partitioned or quadruple -partitioned way in the liquid crystal panel bearing a large screen size and high resolution. In operation, upon receipt of input signals from the outside, the main PCB 340 processes the input signals by way of a built-in timing controller, and generates picture data and various kinds of control signals. The main PCB 340 transmits part of the picture data and control signals to the first source driver PCB 310 via the first and second source FPCs 350 and 360 while transmitting part of the picture data and control signals to the second source driver PCB 320 via the third and fourth source FPCs 370 and 380. The main PCB 340 generates power and various kinds of control signals for driving gate driver IC TABs attached to the gate driver PCB 330, and transmits them to the gate driver PCB 330 via the first and second gate FPCs 390 and 400.

In case the liquid crystal panel is driven in a double-partitioned way, the odd-numbered picture data R2n-1, G2n-1 and B2n-1 generated at the main PCB 340 are transmitted to the first source driver PCB 310 via the first and second source FPCs 350 and 360, whereas the even-numbered picture data R2n, G2n and B2n are transmitted to the second source driver PCB 320 via the third and fourth FPCs 370 and 380. Fig. 5 illustrates the sequence of displaying picture data at the pixels of the liquid crystal panel.

By contrast, as shown in Fig. 6, in case the liquid crystal panel is driven in a quadruple-partitioned way, the first source FPC 350 transmits the picture data and control signals generated from the main PCB 340 to the first source driver PCB 310 to drive the source driver IC TAB attached thereto corresponding to the A portion of the liquid crystal panel. The second source

FPC 360 transmits the picture data and control signals generated from the main PCB 340 to the first source driver PCB 310 to drive the source driver IC TAB attached thereto corresponding to the B portion of the liquid crystal panel. The third source FPC 370 transmits the picture data and control signals generated from the main PCB 340 to the second source driver PCB 320 to drive the source driver IC TAB attached thereto corresponding to the C portion of the liquid crystal panel. The fourth source FPC 380 transmits the picture data and control signals generated from the main PCB 340 to the second source driver PCB 320 to drive the source driver IC TAB attached thereto corresponding to the D portion of the liquid crystal panel. Furthermore, the first gate FPC 390 transmits the power and control signals generated from the main PCB 340 to the gate driver PCB 330 to drive the gate driver IC TAB attached thereto corresponding to the A and B portions of the liquid crystal panel. The second gate FPC 400 transmits the power and control signals generated from the main PCB 340 to the gate driver PCB 330 to drive the gate driver IC TAB attached thereto corresponding to the C and D portions of the liquid crystal panel.

The structure in that the main PCB 340 is connected to the first source driver PCB 310 via the first and second source FPCs 350 and 360 while being connected to the second source driver PCB 320 via the third and fourth FPCs 370 and 380 is made to supply picture data without signal delay in the liquid crystal panel bearing a screen size of 20 inch or more, and high resolution. As described earlier, even in the presence of the main PCBs 240 to 242 shown in Fig. 3, signal delay or distortion is liable to be generated due to the delay factor intrinsic to the RC in the process of interconnecting the PCBs by way of the FPCs 260 and 270. Consequently, the signals applied to the source driver PCBs 210 and 220 are not timing-controlled in a stable manner so that setting and holding of the picture data become to be inappropriate for displaying, resulting in serious display failure accompanied with screen noise and line defect. In view of such a problem, the main PCB 340 is formed with a staple shape such that it is connected to the first source driver PCB 310 via the first and second source FPCs 350 and 360 while being connected to the second source driver PCB 320 via the third and fourth FPCs 370 and 380. Furthermore, the main PCB 340 is designed in consideration of intersignal coupling, noise and EMI such that it can supply signals in the range of tolerance to the source driver PCBs 310 and 320 having space for mounting driver IC TABs, signal lines to be supplied to the drive IC TABs, resistors and condensers for supplying appropriate bias to various signal voltages.

Particularly, in case the liquid crystal panel is driven in a quadruple-partitioned way, the problems of intersignal coupling, noise and EMI are made to be extremely serious. That is, in the top area of the liquid crystal panel, the source driver IC TABs attached to the source driver PCB 310 are differentiated in driving the A and B portions of the liquid crystal panel, and the number of signal lines for transmitting the different picture data and control signals to the respective IC TABs amounts to several tens. Similarly, in the bottom area of the liquid crystal panel, the source driver IC TABs for driving the C and D portions of the liquid crystal display panel are also differentiated, and the number of signal lines for supplying the different picture data and control signals amounts to several

tens. Therefore, it is necessary that the main PCB 340 should be connected to the first source driver PCB 310 via the first and second source FPCs 350 and 360 while being connected to the second source driver PCB 320 via the third and fourth FPCs 370 and 380. In this structure, the main PCB 340 can supply signals in the range of tolerance to the source driver PCBs 310 and 320. Furthermore, the source driver PCBs 310 and 320 are structured to have a sufficient space for receiving the driver IC TABs, the signal lines, and resistors or condensers for giving bias to the respective signal voltages in an appropriate manner. The top and bottom portions of the staple-shaped main PCB 340 have an axial length amounting to one second or more of the liquid crystal panel. The second source FPC 360 and the fourth source FPC 380 interconnecting the first and second source driver PCBs 310 and 320 are positioned at the area that is less than one second of the entire axial length of the top and bottom portions of the main PCB 340 from the side portion thereof. The first source FPC 350 and the third source FPC 370 interconnecting the first and second source driver PCBs 310 and 320 are positioned at the area that is one second or more of the entire axial length of the top and bottom portions of the main PCB 340 from the side portion thereof. In this structure, the possible problems of intersignal coupling, noise, and EMI can be prevented in an efficient manner.

As described above, in the liquid crystal panel with a dual bank typed PCB module according to an embodiment of the present invention, the source driver is partitioned into two parts and installed at the rear of the liquid crystal display module up and down to supply the picture data to the liquid crystal display module. In driving the liquid crystal panel in a double or quadruple-partitioned way, the staple-shaped main PCB 340 minimizing signal delay and distortion is used. Accordingly, such a main PCB can be well adapted for driving the liquid crystal panels with a large screen and high resolution.

[Effect of the invention]

As described above, in driving the liquid crystal panel with a large screen and high resolution, because the main PCB, which generates various data and control signals and supplies them to the source driver PCB and gate driver PCB via the FPCs, respectively by using the timing controller, when viewed from the front side has the staple-shaped shaped, the RC delay, intersignal coupling, noise, and EMI is decreased and distortion is reduced.

In partical, in according to the present invention, because the signal delay and distortion of driving signals for the liquid crystal panel with the large screen size and high resolution is reduced, the main PCB can be well adapted for driving 20 inch or more wide-screened high resolution liquid crystal panel as well as square-shaped liquid crystal panels.